Abstract of the Disclosure

The present invention is related to a method for forming a storage node of a semiconductor device. The method includes the steps of: (a) forming a plurality of bit line patterns, each including a wire and a hard mask sequentially stacked on a surface of a substrate structure; (b) sequentially forming a first barrier layer and a first inter-layer insulation layer along a profile containing bit line patterns until filling spaces between the bit line patterns; (c) etching the first inter-layer insulation layer until a partial portion of the first inter-layer insulation layer remains on each space between the bit line patterns; (d) forming a second barrier layer on the first inter-layer insulation layer and the first barrier layer; and (e) etching the first and the second barrier layers and the remaining first inter-layer insulation layer to expose a surface of the substrate structure disposed between the bit line patterns.